

Listing of the Claims

This Listing of the Claims will replace all prior versions and listings of claims in this application.

Claims 1 – 6 (Cancelled)

7. (New) A method of forming a graded junction in a semiconductor substrate utilizing an integrated circuit fabrication technique that is characterized by a minimum geometry feature size, the semiconductor substrate having a first conductivity type, the method comprising:

forming a patterned mask on the upper surface of the semiconductor substrate, the patterned mask having a first mask opening formed therein that exposes a first surface region of the semiconductor substrate such that, when a dopant is introduced into the first substrate surface region through the first mask opening, a primary dopant junction is formed between a resulting first dopant region and the semiconductor substrate, the first surface region having dimensions that are greater than the minimum geometry feature size, the patterned mask further having a second mask opening formed therein that exposes a perimeter surface region of the semiconductor substrate, the perimeter surface region being defined around the perimeter of the first surface region and space-apart from the first surface region by a distance that is less than two times (2x) the lateral diffusion length of the dopant from the primary dopant junction during a thermal diffusion step applied to the semiconductor substrate;

introducing the dopant through the first mask opening into the first surface region of the semiconductor substrate to form a primary dopant region, the primary dopant region having a second conductivity type that is opposite the first conductivity type, the primary dopant region having a first dopant concentration, the perimeter of the primary dopant region defining the primary dopant junction between the primary dopant region and the semiconductor substrate;

simultaneously with forming the primary dopant region, introducing the dopant through the second mask opening into the perimeter surface region of the semiconductor substrate to form a perimeter dopant region having the second conductivity type in the semiconductor substrate around the perimeter of the primary dopant region such that the perimeter dopant region is spaced-apart from the primary dopant junction by a distance that is less than two times (2x) the lateral diffusion length of the primary junction during the thermal diffusion step, the

perimeter dopant region having a second dopant concentration that is less than the first dopant concentration; and

performing the thermal diffusion step such that the dopant in the primary dopant region and the dopant in the perimeter dopant region diffuse to merge to provide a single graded dopant region that includes an interior portion that has a first dopant gradient with a first maximum dopant concentration and a perimeter portion that is contiguous with the interior portion and has a second dopant gradient with a second maximum dopant concentration that is less than the first maximum dopant concentration.

8. (New) A method of forming a graded junction in a semiconductor substrate utilizing an integrated circuit fabrication technique that is characterized by a minimum geometry feature size, the semiconductor substrate having a first conductivity type, the method comprising:

forming a patterned mask on an upper surface of the semiconductor substrate, the patterned mask including a first mask opening that exposes a first upper surface area of the semiconductor substrate, the first mask opening having a feature size that is greater than the minimum geometry feature size, and a second mask opening that defines a perimeter upper surface area of the semiconductor substrate that surrounds and is spaced-apart from the first upper surface area by a distance that is less than two times (2x) the lateral diffusion length of a dopant having a second conductivity type that is opposite the first conductivity type in the semiconductor substrate during a thermal diffusion step applied to the semiconductor substrate, the second opening having the minimum geometry feature size;

in a single ion implant step, utilizing the patterned mask to implant the dopant through the first mask opening into the first upper surface area of the semiconductor material to define a primary dopant region therein such that the primary dopant region defines a primary dopant junction between the primary dopant region and the semiconductor substrate, and through the second mask opening into the perimeter upper surface area of the semiconductor material to define a perimeter dopant ring therein that is spaced-apart from the primary dopant junction; and

performing the thermal diffusion step such that the dopant in the primary dopant region and in the perimeter dopant ring diffuses to merge to provide a single graded dopant region that includes an interior portion that has a first dopant gradient with a first maximum dopant concentration and a perimeter portion that is contiguous with the interior portion and has a

second dopant gradient with a second maximum dopant concentration that is less than the first maximum dopant concentration.

9. (New) A method of forming a graded junction in a semiconductor substrate utilizing an integrated circuit fabrication technique that is characterized by a minimum geometry feature, the semiconductor substrate having a first conductivity type, the method comprising:

forming a patterned mask on an upper surface of the semiconductor substrate, the patterned mask including a first mask opening that exposes a first upper surface area of the semiconductor substrate that has feature size greater than the minimum feature size and a second set of mask openings that define a plurality of quadrilateral island areas on the upper surface of the semiconductor substrate, the island areas being disposed around and spaced-apart from the perimeter of the first upper surface area by a distance that is less than two times (2x) the lateral diffusion length of a dopant in the semiconductor substrate during a thermal diffusion step that is part of the integrated circuit fabrication technique, each of the plurality of island areas having the minimum geometry feature;

in a single ion implant step, utilizing the patterned mask to implant the dopant through the first mask opening into the first upper surface area of the semiconductor substrate to define a primary dopant region therein, the primary dopant region defining a primary dopant junction between the primary dopant region and the semiconductor substrate, and through the second set of mask openings into the upper surface island areas of the semiconductor substrate to define a plurality of quadrilateral perimeter dopant islands therein that are spaced-apart from the primary dopant region; and

performing the thermal diffusion step such that dopant in the primary dopant region and dopant in the perimeter dopant islands diffuses to merge to provide a single graded dopant region that includes an interior portion that has a first dopant gradient with a first maximum dopant concentration and a perimeter portion that is contiguous with the interior portion and has a second dopant gradient with a second maximum dopant concentration that is less than the first maximum dopant concentration.